

IN THE CLAIMS:

1-30 (Cancelled)

31. (Currently Amended) A method for testing a memory device having a plurality of data lines, comprising:

latching [[reading]] data present on at least a subset of the plurality of data lines;

masking the latched data associated with at least one data line of the subset;

compressing the masked data to determine ~~determining~~ if the masked data matches a predetermined pattern; and

providing at least a pass signal if the masked data matches the predetermined pattern.

32. (Currently Amended) The method of claim 31, wherein ~~the determining comprises~~ compressing the masked data further comprises determining ~~to determine~~ if each datum of the data matches a predetermined value.

33-37 (Cancelled)

38. (Currently Amended) An apparatus for testing a memory device having a plurality of data lines, comprising:

means for [[reading]] latching data present on at least a subset of the plurality of data lines;

means for masking the latched data associated with at least one data line of the subset;

means for compressing the masked data to determine ~~determining~~ if the data matches a predetermined pattern; and
means for providing at least a pass signal if the data matches the predetermined pattern.

39. (New) The method of claim 31, further comprising:

providing a plurality of latches for latching the data associated with the subset;
providing a plurality of enable signals to the latches; and
disabling latches in the plurality of latches responsive to a deassertion of the associated enable signals.

40. (New) The method of claim 39, wherein disabling the latches further comprises forcing the disabled latches to output a predetermined voltage.

41. (New) The method of claim 40, wherein forcing the disabled latches to output the predetermined voltage further comprises forcing the disabled latches to output a voltage corresponding to a logic 1.

42. (New) The method of claim 40, wherein forcing the disabled latches to output the predetermined voltage further comprises forcing the disabled latches to output a voltage corresponding to a logic 0.

43. (New) The method of claim 39, further comprising:

receiving a latch signal; and

latching the data responsive to the latch signal being asserted in the latches with associated enable signals asserted.

44. (New) The method of claim 43, further comprising bypassing the latch responsive to the latch signal being deasserted.

45. (New) The method of claim 31, further comprising:

providing a plurality of latches for latching the data associated with the subset;

receiving a clock signal and a latch signal; and

latching the data based on a first combination of the latch signal and the clock signal.

46. (New) The method of claim 31, wherein compressing the masked data further comprises performing a NAND Boolean function.

47. (New) The method of claim 31, wherein compressing the masked data further comprises performing a NOR Boolean function.

48. (New) The apparatus of claim 38, wherein the means for masking the latched data further comprises means for disabling the latching means responsive to deassertions of enable signals associated with the data lines in the subset.

49. (New) The apparatus of claim 48, wherein the means for disabling further comprises means for forcing the disabled latches to output a predetermined voltage.

50. (New) The apparatus of claim 49, wherein the predetermined voltage corresponds to a logic 1.

51. (New) The apparatus of claim 49, wherein the predetermined voltage corresponds to a logic 0.

52. (New) The apparatus of claim 38, further comprising means for bypassing the latching means responsive to a deassertion of a latch signal:

53. (New) The apparatus of claim 38, wherein the means for compressing the masked data further comprises means for performing a NAND Boolean function.

54. (New) The apparatus of claim 38, wherein the means for compressing the masked data further comprises means for performing a NOR Boolean function.